University of Thi-Qar
Electrical and Electronic Engineering Department   lecture Six
.Second year, Electronic ı, 2016-2017   by: Abdulgaffar S. M

Voltage-Multiplier Circuits

Basic Concepts:

Diodes and capacitors can be connected in various configuration to produce filtered, rectified voltages that are integer multiples of the peak value of an input sine wave. The principle of operation of these circuits is similar to that of the clamping circuits discussed previously. By using a transformer to change the amplitude of an ac voltage before it is applied to a voltage multiplier, a wide range of the dc levels can be produced using this technique. One advantage of a voltage multiplier is that high voltages can be obtained without using a high-voltage transformer.

Voltage Doubler:

1. Half-Wave Voltage Doubler:

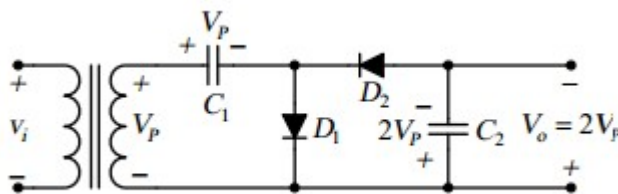Figure 6-1 shows a half-wave voltage doubler circuit.

Fig. 6-1

Operation:

- During the positive half-cycle,
  $D_1 \, ON \circ D_2 \, OFF \Rightarrow charging \, C_1 \, up \oplus V_P$

- During the negative half-cycle,
  $D_2 \, ON \circ D_1 \, OFF \Rightarrow charging \, C_2 \, up \oplus 2 \, V_P$

- The output (V_o) of the half-wave voltage doubler is

$$V_o = V_{C2} = 2 V_P \qquad [6.1]$$

If a load is connected to the output of the half-wave voltage doubler , the voltage across capacitor C_2 drops during the positive half-cycle (at the input) and the capacitor is recharged up to $2 V_P$ During the negative half-cycle. The output waveform across capacitor C_2 is that of a haif-wave signal filtered by a capacitor filter.

1

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The peak inverse voltage (*PIV*) rating of each diode in the half-wave voltage doubler circuit must be at least $2V_P$

2. **Full-Wave Voltage Doubler**:
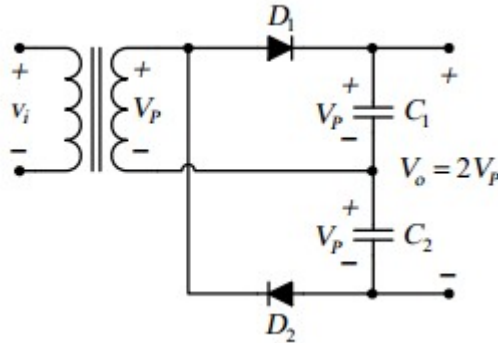   Figure 6-2 shows a full-wave voltage doubler circuit.

:Operation   **Fig. 6-2**

- During the positive half-cycle,
  $D_1 ON \circ D_2 OFF \Rightarrow charging\ C_1\ up \oplus V_P$

- During the negative half-cycle,
  $D_2 ON \circ D_1 OFF \Rightarrow charging\ C_2\ up \oplus V_P$

- The output (V_o) of the half-wave voltage doubler is

$$V_o = V_{C1} = V_{C2} = \oplus\ 2V_P \qquad [6.2]$$

If load current is drawn from the full-wave voltage doubler circuit, the voltage across the capacitors C_1 and C_2 is the across a capacitor fed by a full-wave rectifier. One difference is that of C_1 and C_2 in series, which is less than capacitance of either C_1 and C_2 alone. The lower capacitor value will provide poorer filtering action than the single-capacitor filter circuit.

The peak inverse voltage (*PIV*) across each diode is $2V_P$, as it is for filter capacitor circuit.

2

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Voltage Tripler and Quadrupler:

Figure 6-3 shows an extension of the half-wave doubler, which develops three and four times the peak input voltage. It should be obvious from the pattern of the circuit connection how additional diodes and capacitors may be connected so that the output voltage may also be five, six, seven, and so on, times the basic peak voltage(V_P).
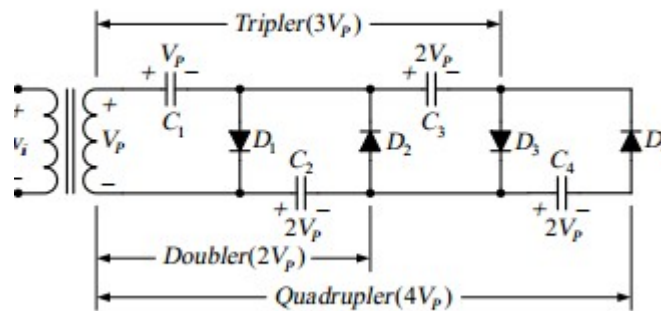

Fig. 6-3

Operation:

- During the positive half-cycle,
  $D_1 ON \circ D_2, D_3, D_4 OFF \Rightarrow charging\ C_1\ up \oplus V_P$

- During the negative half-cycle,
  $D_2 ON \circ D_1, D_3, D_4 OFF \Rightarrow charging\ C_2\ up \oplus 2V_P$

- During the next positive half-cycle,
  $D_1, D_3 ON \circ D_2, D_4 OFF \Rightarrow C_2\ charges\ C_3\ up \oplus 2V_P$

- During the next negative half-cycle,
  $D_2, D_4 ON \circ D_1, D_3 OFF \Rightarrow C_3\ charges\ C_4\ up \oplus 2V_P$

- The voltage across the combination of C_1 and C_3 is $3V_P$ and the across C_2 and C_4 is $4V_P$.

  The PIV rating of each diode in the circuit must be at least $2V_P$.

Exercises:

1. A certain doubler has 35V rms on its input. What is the output voltage? Sketch the circuit, indicating the output terminals and PIV for the diode.

2. Repeat exercise 1 for a voltage tripler and quadrupler.

3

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3. The output voltage of a quadrupler is 620V. what minimum PIV rating must each diode have?