JFET Small-Signal Analysis

Since it has a very high input resistance high input resistance , therefore I_G could be neglected. Hence , I_D could be represented as function of V_{GS} and V_{DS} .

$I_D = f(V_{GS}, V_{DS})$,

$$I_D = g_m V_{GS} + \frac{1}{r_d} V_{DS}$$

Where $g_m = \left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{V_{DS}=const.}$ mutual-conductance or transconductance

$\frac{1}{r_d} = \left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{V_{DS}=const.}$ where r_d drain-resistance $r_d = \frac{1}{y_{of}} = \frac{V_{DS}}{I_D}$

$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D=const.} = g_m r_d$ amplification factor

Also $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$

Where $g_{mo} = \frac{2 I_{DSS}}{V_p}$ the value of g_m of $V_{GS} = 0$

Note:

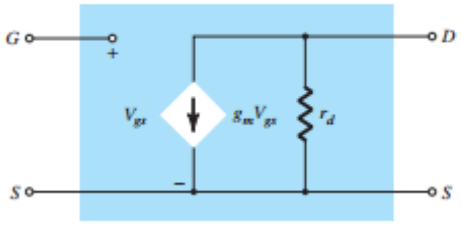
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$g_m = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{DS}=const.}$$

$$g_m = \frac{2 I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_{mo} = \frac{2I_{DSS}}{V_p}$$

FET AC Equivalent Circuit:



I_b situations where r_d is ignored (assumed sufficiently large to other element of the network to be approximated by an open circuit) , the equivalent circuit whose magnitude is controlled by the signal V_{gS} and parameter g_m clearly a voltage-controlled device.

Common-Source Configuration:

The common-source configuration circuit of Fig. 17-1 includes a source resistor (Rs) that may or may not be bypassed by a source capacitor (Cs) in the ac domain.

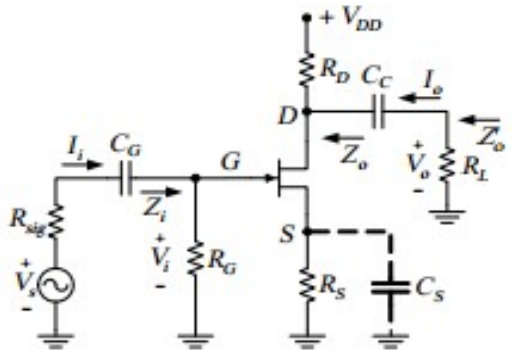


Fig. 17-1

Bypassed (absence of Rs):

For the ac equivalent circuit of Fig. 17-2,

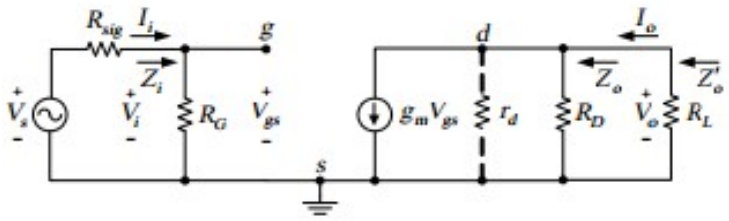


Fig. 17-2

Input impedance:

$$Z_i = R_G$$

Output impedance:

Approximate (neglecting rd);

$$Z_o = R_D \quad for\ rd \geq 10\,R_D$$

$$Z_o = R_L \parallel R_D$$

Exact (including rd);

$$Z_o = R_D \parallel rd$$

$$Z_o = R_L \parallel Z_o = R_L \parallel R_D \parallel rd$$

Voltage gain:

Approximate (neglecting rd);

$$V_O = -g_m V_{gs} (R_L \parallel R_D),$$

$$V_{gs} = V_i,$$

$$A_V = \frac{V_o}{V_i} = -g_m (R_L \parallel R_D)$$

$$A_{Vs} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s} = A_V \cdot \frac{Z_i}{Z_i + R_{sig}}$$

Exact (including rd);

$$A_V = -g_m (R_L \parallel R_D \parallel rd)$$

Current gain:

$$A_i = \frac{I_o}{I_i} = -A_V \cdot \frac{Z_i}{R_L}$$

Phase relationship:

The negative sign in the resulting equation for A_v reveals that a 180_o phase shift occurs between the input and output signals.

Unbypassed (include of R_S):

For the approximate ac equivalent circuit ($r_d \approx \infty\Omega$) of Fig. 17-3,

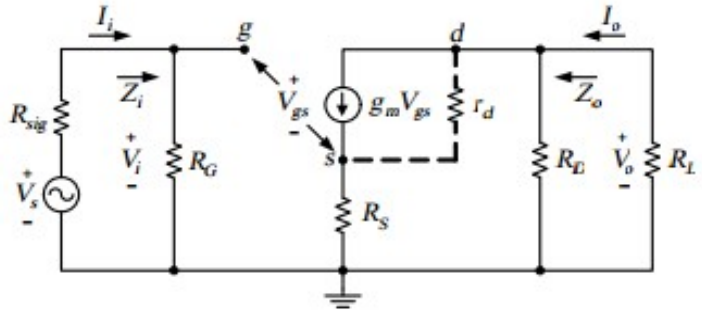


Fig. 17-3

Output impedance:

$For\ V_i = 0\,V,\ I_o = I_{R_D} = g_m V_{gs}, with\ V_{gs} = -V_{R_s}, at\ V_i = 0\,V = -I_o = I_{R_D}(R_s,$

so that $I_o = I_{R_D} = -g_m(I_o = I_{R_D})R_S, \Rightarrow I_o(1 = g_m R_S) = -I_{R_D}(1 = g_m R_S),$

and $I_o = -I_{R_D}$

Since $V_o = -I_{R_D} R_D, then\ V_o = -(-I_o)R_D = I_o R_D,$ and

$$Z_o = \frac{V_o}{I_o} = R_D$$

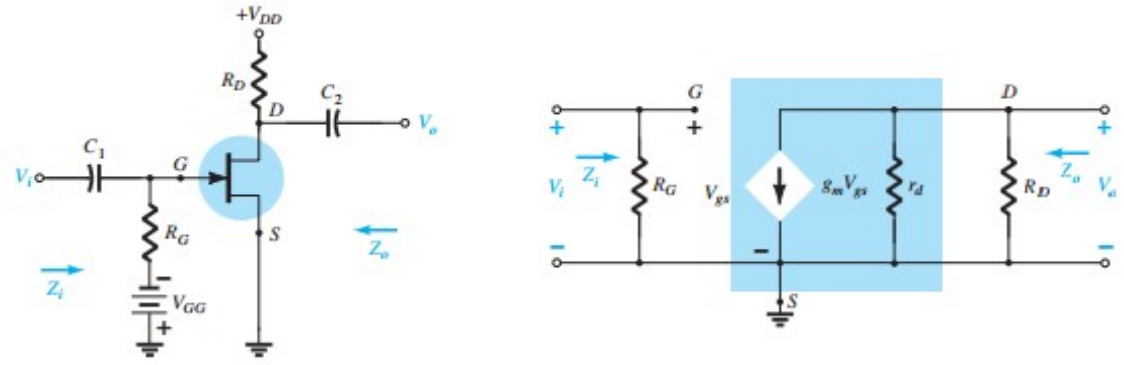
Voltage gain:

$$V_o = -g_m V_{gs} (R_l \parallel R_D)$$

$$V_{gs} = V_g - V_s = V_i - g_m V_{gs} R_s \Rightarrow V_i = (1 + g_m R_s) V_{gs}$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m (R_l \parallel R_D)}{1 + g_m R_s}$$

Fixed-Bias Configuration:



From equivalent circuit

$Z_i = R_G$ High (10μΩ)

$Z_o = R_D \parallel r_d$

R_D ($rd \geq 10 R_D$)

$$A_V = \frac{V_o}{V_i} = -g_m (rd \parallel R_D)$$

$$= -g_m rd \quad (rd \geq 10 R_D)$$

Common-Drain (Source-Follower) Configuration:

The common-drain (source-follower) configuration circuit is shown in Fig. 17-4.

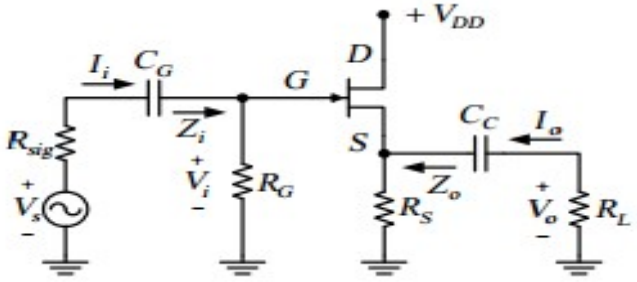


Fig. 17-4

For the ac equivalent circuit of Fig. 17-5,

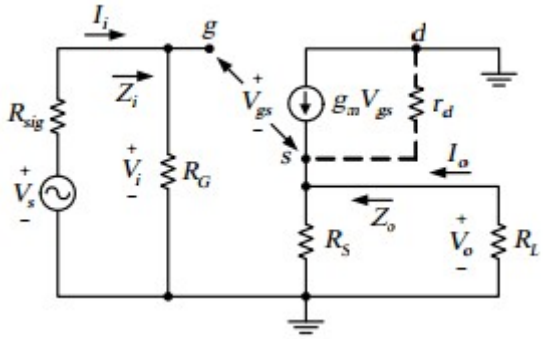


Fig. 17-5

Input impedance:

$Z_i = R_G$ [high]

Output impedance:

For $V_i = 0\,V$, $I_o = g_m V_{gs} + I_{r_d} = I_{R_s} + V_o / r_d = V_o / R_s$

$I_o = V_o / 1/r_d = 1/R_s - g_m V_{gs}$, with

$V_{gs} = -V_o$, at $V_i = 0\,V$ $I_o = V_o / 1/r_d = 1/R_s = g_m$,

$$\left(1+g_m\right)$$
$$\left(1+r_d\right)\|\left(1+R_s\right)\|\left(1+\right)$$
$$Z_o=V_o/I_o\|1+$$

$$Z_o=r_d\|R_s\|\left(1+g_m\right) \qquad \text{[low]}$$

$$Z_o=R_s\|\left(1+g_m\frac{R_s}{1+g_mR_s}\right) \text{ for } r_d\geq 10R_s$$

Voltage gain:

$$V_o=-g_mV_{gs}\left(R_l\|R_s\|r_d\right),$$

$$V_{gs}=V_g-V_s=V_i-V_o=V_i-g_mV_{gs}\left(R_l\|R_s\|r_d\right)\Rightarrow V_i=\left(1+g_m\left(R_l\|R_s\|r_d\right)\right)V_{gs}$$

$$A_v=\frac{V_o}{V_i}=\frac{g_m\left(R_l\|R_s\|r_d\right)}{1+g_m\left(R_l\|R_s\|r_d\right)} \qquad \text{[less than 1]}$$

$$A_v=\frac{V_o}{V_i}=\frac{g_m\left(R_l\|R_s\right)}{1+g_m\left(R_l\|R_s\right)} \text{ for } r_d\geq 10R_s$$

Phase relationship:

V_o and V_i are in-phase.

Common-Gate Configuration:

The common-gate configuration circuit is shown in Fig. 17-6.

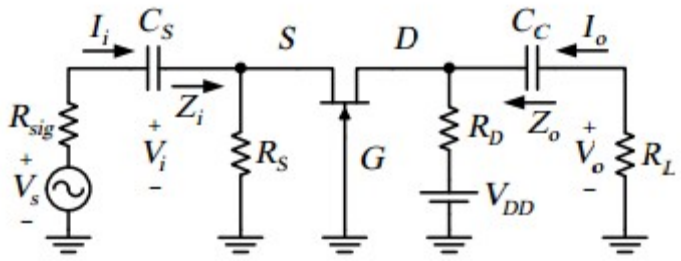


Fig. 17-6

For the approximate ac equivalent circuit ($r_d \approx \infty\Omega$) of Fig. 17-7,

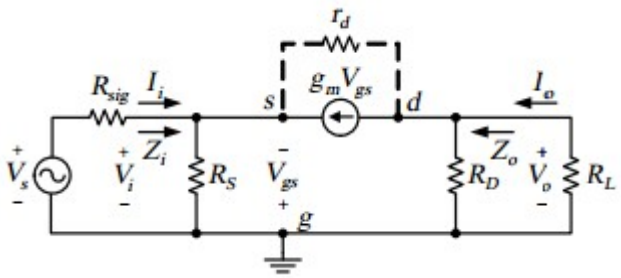


Fig. 17-7

Input impedance:

$$Z_o = R_s \parallel \frac{1}{g_m} \frac{R_s}{1 + g_m R_s} \quad \text{[low]} \qquad \text{(Derive)}$$

Output impedance:

$$Z_o = R_D$$

Voltage gain:

$$V_o = -g_m V_{gs} (R_l \parallel R_D), \qquad V_{gs} = -V_i$$

$$A_v = \frac{V_o}{V_i} = g_m (R_l \parallel R_D)$$

Phase relationship:

V_o and V_i are in-phase.

Example 17-1 (Analysis):

For the JFET amplifier circuit of Fig. 17-8 with parameter $g_m = 2.2$ mS, determine: Z_i, Z_o, , Z_o ' $A_\varpi = V_o/V_i$, $A_i = I_o/I_i$, $A_v = V_o / V_s$ and $V_o = 0$. *Assume* $r_d \geq 10 R_D$.

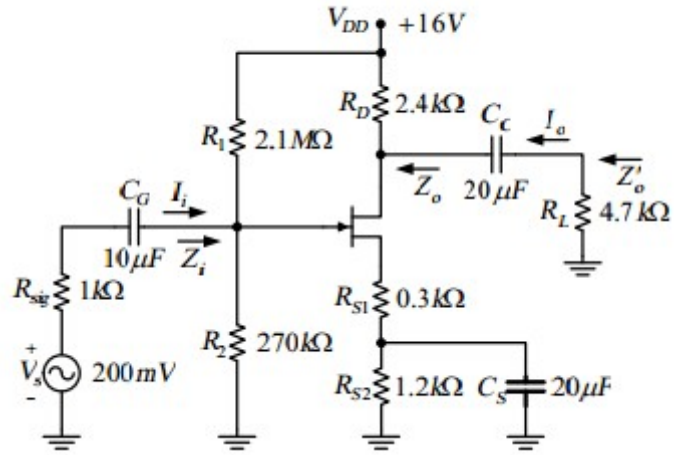


Fig. 17-8

Solution:

$$Z_i = R_1 \parallel R_2 = 2.1\,M \parallel 0.27\,M = 239\,k\Omega$$

$$Z_i = R_1 = 2.4\,k\,\Omega,\ Z_o = R_L \parallel R_D = 4.7\,k \parallel 2.4\,k = 1.59\,k\,\Omega.$$

$$A_v = \frac{-g_m (R_l \parallel R_D)}{1 + g_m R_{s1}} = \frac{-(2.2\,m)(1.59\,k)}{1 + (2.2\,m)(0.3\,k)} = -2.11.$$

$$A_i = -A_V \cdot \frac{Z_i}{R_L} = \frac{-(12.11)(239\,k)}{4.7\,k} = 107.$$

$$A_{Vs} = A_V \cdot \frac{Z_i}{Z_i + R_{sig}} = \frac{(-2.11)(239\,k)}{4.7\,k} = -2.10 \approx A_V.$$

$$V_o = A_{Vs} V_s = -2.10(200\,m) = 420\,mV.$$

Example 17-2 (Design):

Complete the design of the JFET amplifier circuit shown in Fig. 17-9 to have a voltage gain magnitude of 17.5 dB, using a relatively high level of g_m for this device defined at $V_{GSQ} = V_P/4$. Assume $_d > 10R_D$.

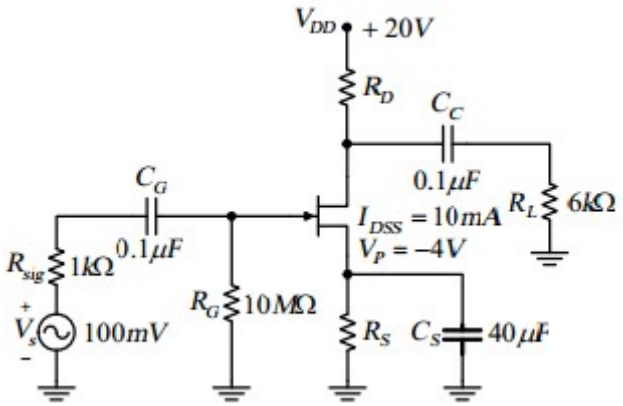


Fig. 17-9

Solution:

$V_{GsQ} = V_P = 4 = -4 = 4 = -1\,V$,

$g_m = \frac{2\,I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right) = \frac{2(10\,m)}{4}\left(1-\frac{-1}{-4}\right) = 3.75\,mS$,

$G(dB) = 20\log_{10}(A_v) \Rightarrow 17.5 = 2020\log_{10}(A_v) \Rightarrow A_v = 7.5$,

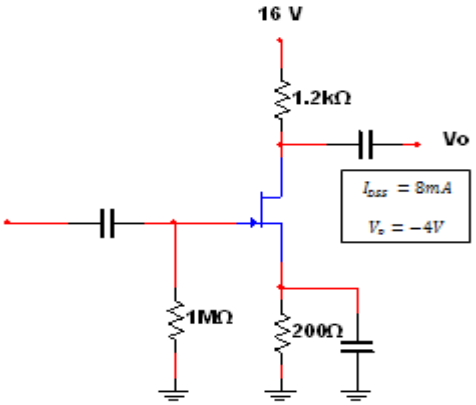
$A_v = g_m(R_L \parallel R_D) \Rightarrow 7.5 = 3.75\,m(6\,k \parallel R_D) \Rightarrow R_D = 3\,k\,\Omega$.

$I_{DQ} = I_{DSS}\left(1-\frac{V_{GSQ}}{V_P}\right)^2 = 10\,m\left(1-\frac{-1}{-4}\right)^2 = 5.625\,mA$,

$V_{GSQ} = -I_{DQ}R_s \Rightarrow 1 = -5.625\,m\,R_s \Rightarrow R_s = 178\,\Omega$.

Example:

Calculate the circuit factor A_v and R_o (assume r_d can be neglected)



Solution:

$$V_{GSQ} = -0.94\,V$$

$$g_{mo} = \frac{2\,I_{DSS}}{V_P} = \frac{2(8\,m)}{-4} = 4\,mS$$

$$g_m = g_{mo}\left(1-\frac{V_{GS}}{V_P}\right) = 4\,mS\left(1-\frac{-0.94\,V}{-4\,V}\right) = 3.06\,mS$$

$$A_V = -g_m R_D = -\left(\frac{3.06\,mS}{}\right)(1.2k) = -3.67$$

$$R_i = R_G = 1\,M\,\Omega$$

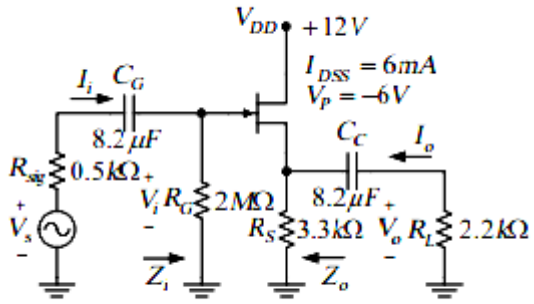
$$R_o = R_D = 1.2\,k\,\Omega$$

$$r_m = \frac{1}{g_m} \Rightarrow A_V = -g_m R_D = \frac{-R_D}{r_m}$$

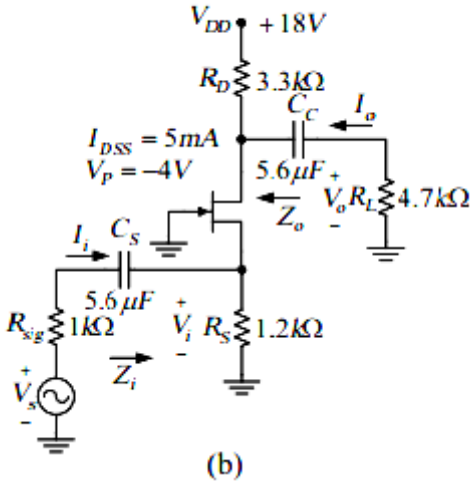
Exercises:

1. For each one of the circuits shown in Fig. 17-10, determine:

(a) V_{GS}, and g_m. (b) Z_i, and Z_o. (c) $A_v = \frac{V_o}{V_i}$ $A_i = \frac{I_o}{I_i}$



(a)



(b)

2. Choose the values of R_D, R_S, and R_L for the JFET amplifier circuit of Fig. 17-11 that will result in a gain of 18.062 dB. Assume that I_{DSS} = 8 mA, V_P = −4 V, $r_d \approx \infty\ \Omega$, V_{DQ}/V_{DD} = 0.375, and I_{DQ}/I_{DSS} = 0.25. Calculate $A_{vs} = V_o / V_s$, and sketch V_o.

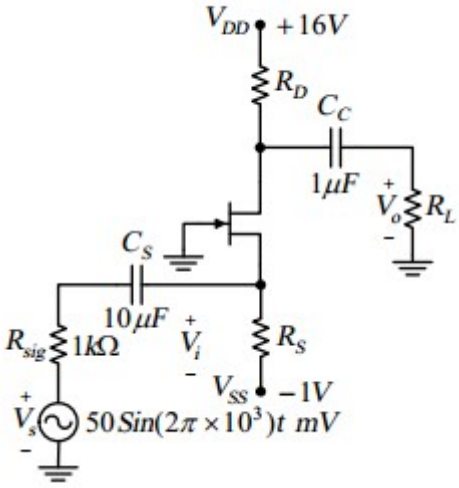


Fig. 17-11