Field-Effect Transistors (FETs)

Basic Definitions:

The FET is a semiconductor device whose operation consists of controlling the flow of current through a semiconductor channel by application of an electric field (voltage).

There are two categories of FETs: the **junction field-effect transistor** (JFET) and the **metal-oxide-semiconductor field-effect transistor** (MOSFET). The MOSFET category is further broken-down into: **depletion** and **enhancement** types.

A Comparison between FET and BJT:

- FET is a **unipolar** device. It operates as a **voltage-controlled** device with either electron current in an **n-channel** FET or hole current in a **p-channel** FET.
- BJT made as **npn** or as **pnp** is a **current-controlled** device in which both electron
  current and hole current are involved.
- The FET is smaller than a BJT and is thus for more popular in **integrated circuits**
  (ICs).
- FETs exhibit much higher **input impedance** than BJTs.
- FETs are more **temperature stable** than BJTs.
- BJTs have large **voltage gain** than FETs when operated as an amplifier.
- The BJT has a much higher **sensitivity** to changes in the applied signal (faster **response**) than a FET.

Junction Field-Effect Transistor (JFET):

The basic construction of n-channel (p-channel) JFET is shown in Fig. 15-1a (b). Note that the major part of the structure is n-type (p-type) material that forms the channel between the embedded layers of p-type (n-type) material. The top of the n-type (p-type) channel is connected through an ohmic contact to a terminal referred to as the **drain** "D", while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the **source** "S". The two p-type materials are connected together and to the **gate** "G" terminal.

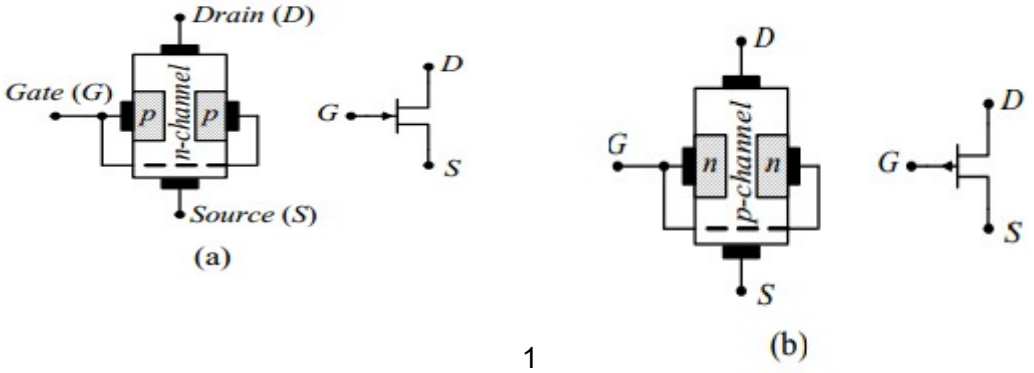
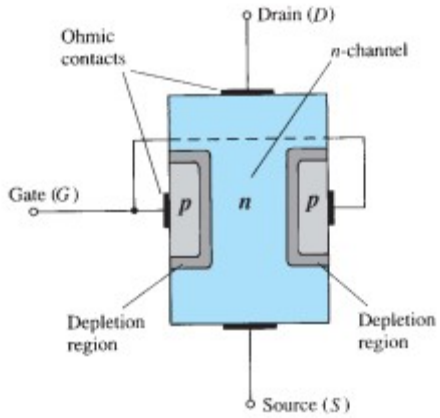
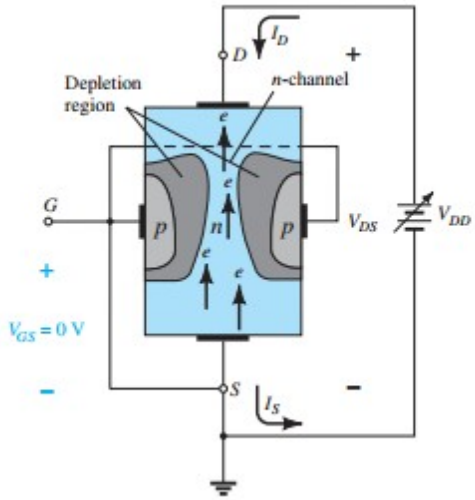
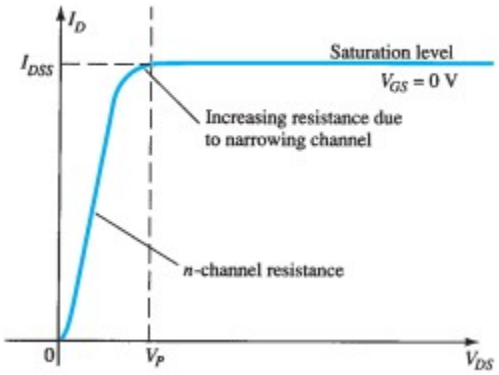


Fig. 15-1

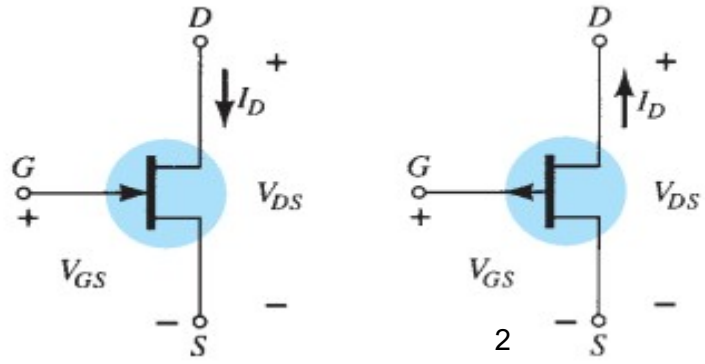




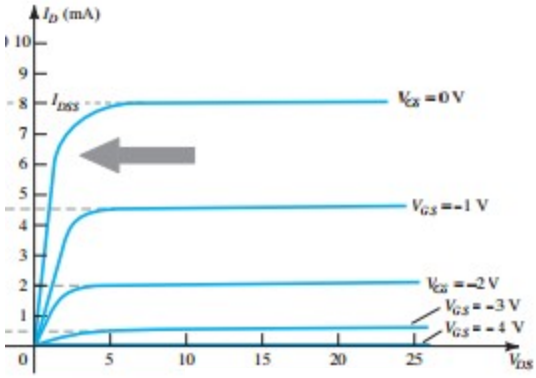
$V_{GS} = 0\,V$, V_{GS} *same positive value*

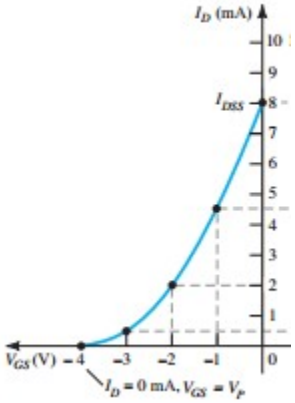


Schematic Symbol of JFET



n-channel JFET p-channel JFET





Control variable

↓

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad \equiv I_C = f(I_B) = \beta I_B$$

↑ ↑ constant

$$1 - \frac{V_{DS}}{V_P}$$

$$r_d = \frac{r_o}{}$$

r_d is resistance at a pariticular level of V_{GS}

Important Terms:

1- Shorted-gate drain current I_{DSS}

2- Pinch off voltage V_P

3- Gate-source cut off voltage [$V_{GS(off)}$]

1) Shorted-gate drain current(I_{DSS}) it is the drain current with source short-circuited to gate $V_{GS} = 0$ and drain voltage V_{DS} equal to pinch off voltage.

Note:

I- since I_{DSS} is measured under shorted gate conditions, it is the maximum drain current that you can get with normal operation JFET.

II- There is a maximum drain voltage($V_{DS\,max}$) that can be applied to a FET would break down.

III- The region between V_P and $V_{DS\,max}$ (break down) is called constant-current region or active region.
As long as V_{DS} is kept within this range , I_P will remain constant value of V_{GS} .

2) Pinch off voltage V_P . it is minimum drain-source voltage at which the drain current essentially becomes constant.

3) Gate-source cut off voltage [$V_{GS(off)}$]. It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.

Notes:

I- It is interesting to note that V_{GS} off will always have the same magnitude value as V_P . For example $V_P = 6V$ then $V_{GS(off)} = -6V$. Since two values are always equal and opposite .

II-There is a distinct difference between V_P and $V_{GS(off)}$. Note that V_P is the value of V_{DS} that causes the JFET to become a constant current device. It is measured at $V_{GS} = 0V$ and will have a constant drain current= I_{DSS} , However $V_{GS(off)}$ is the value of V_{GS} that causes I_D to drop nearly zero.

Difference between JFET and Bipolar transistor:

The JFET differs from an ordinary or bipolar transistor in the following ways:

I- In a JFET, there is only one type of carrier, holes in p-type channel and electrons in n-type channel. For this reason it is also called unipolar transistor. However in an ordinary transistor both holes and electrons and called bipolar transistor.

II- As the input circuit (gate to source) of a JFET is reverse biased , therefore , the device has high input impedance. However the input circuit of an ordinary transistor is forward biased and hence has low input impedance.

III- As the gate is reverse biased, therefore it carries very small current. Obviously JFET is just like a vacuum tube where control grid (corresponding to gate in JFET) carries extremely small current and input voltage controls the output current. For this reason ,JFET is essentially a voltage driven device. However, ordinary transistor is a current operated device input current controls the output current.

IV- A bipolar transistor use a current into its base to control a large current between collector and emitter whereas a JFET use voltage on the gate (=base) terminal to control the current between drain(=collector) and source(=emitter). Thus a bipolar transistor gain is characterized as a trans conductance , the ratio of change in output current (drain current) to the input (gate) voltage.

V- In JFET, there are no junction as an ordinary transistor. The conduction is through an n-type or p-type semi-conductor material. For this reason noise level in JFET is very small.

Disadvantage of JFET:

It has a smaller gain and bandwidth than bipolar transistor.

Advantage of FET:

1- It's operation depends upon the flow of majority carriers only. Therefore it is unipolar.
2- It requires less space in integrated circuit and is very simple to fabricate.
3- It has high input impedance (of the order of MΩ)
4- It is less noisy than value a bipolar transistor.
5- It has no offset voltage at $I_D = 0$, so it makes an excellent chopper.
6- It has good thermal stability.

Applications:

The principle application is in LSI digital array.

FET Static Characteristics:

For n-channel FET, V_{DS} and I_D are positive (+ve) while V_{GS} and I_G are negative(-ve).

For p-channel FET, V_{DS} and I_D are negative(-ve). While V_{GS} and I_G are positive (+ve)

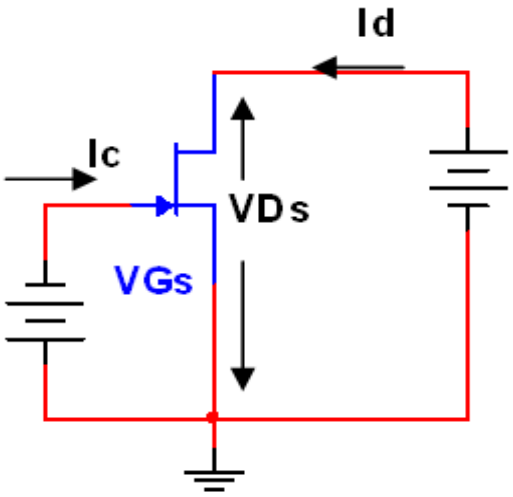
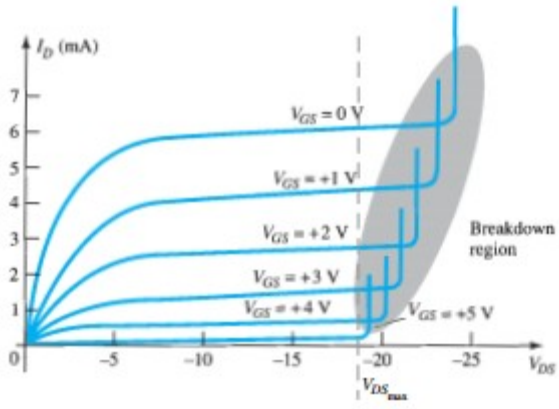


Fig. common-source drain characteristics of a n-channel FET.

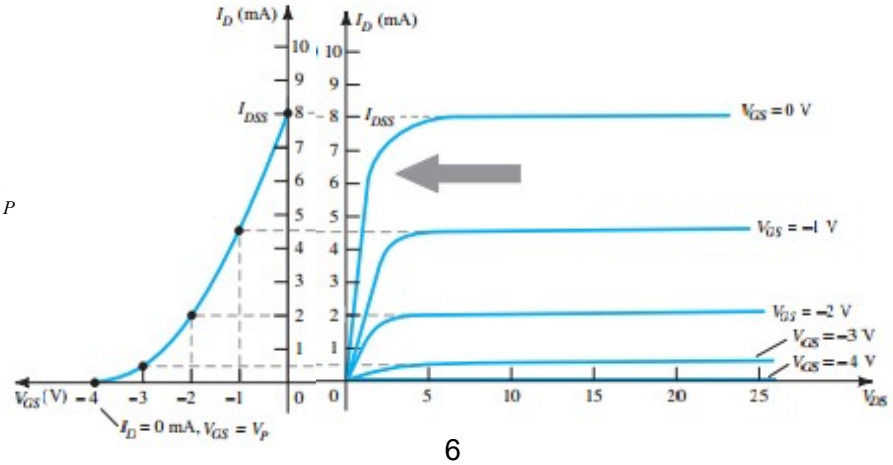


when $V_{GS} = 0$

$I_D = I_{DSS}$

when $V_{GS} = V_P$

$I_D = 0$



The characteristics are described by

$$I_D = K\left(1-\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}} V_{DS}$$ output C/C

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}\,2}$$ transfer

C/CS

Where:

V_P: *pinch off voltage (the drain voltage that causes I_D approach a constant value)*

K: *constant*

I_{DSS}: *maximum drain current occurs when* $V_{GS} = 0$, $I_{DSS} = I_D$

The equation which described the transfer C/CS is called Shockley's equation.

Region before V_P behaves as an ohmic resistance for small V_{DS} and as constant current device for large V_{DS}. Beyond V_P (also called constant current or constant saturation region).

For $V_{GS} \leq V_P \Rightarrow r_d = \frac{V_{DS}}{I_D}$ drain resistance

Or $r_d = \frac{r_o}{1-\frac{V_{GS}}{V_P}}$ when r_o constant (r_d *when* $V_{GS} = 0$)

$\frac{1}{r_d}$ drain conductance.

Basic Operation of JFET:

- Bias voltages are shown, in Fig. 15-2, applied to an n-channel JFET devise.
- V_{DD} provides a drain-to-source voltage, V_{DS}, (drain is positive relative to source) and supplies current from drain to source, I_D, (electrons move from source to drain).
- V_{GG} sets the reverse-bias voltage between the gate and the source, V_{GS}, (gate is biased negative relative to the source).
- Input impedance at the gate is very high, thus the gate current $I_G = 0$ A.
- Reverse biasing of the gate-source junction produces a depletion region in the n-channel and thus increases its resistance.
- The channel width can be controlled by varying the gate voltage, and thereby, I_D can also be controlled.
- The depletion regions are wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source.

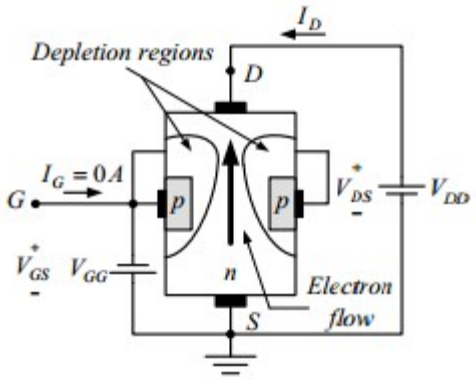


Fig. 15-2

JFET Characteristics:

❖ When $V_{GS} = 0$ V and $V_{DS} < V_P$ (**pinch-off voltage**)*: I_D rises linearly with V_{DS} (**ohmic region**, n-channel resistance is constant), as shown in Fig. 15-3.

- *When V_{DS} is increased to a level where it appears that the two depletion regions would "touch", a condition referred to as pinch-off will result. The level of V_{DS} that establishes this condition is referred to as the pinch-off voltage and is denoted by V_P.*

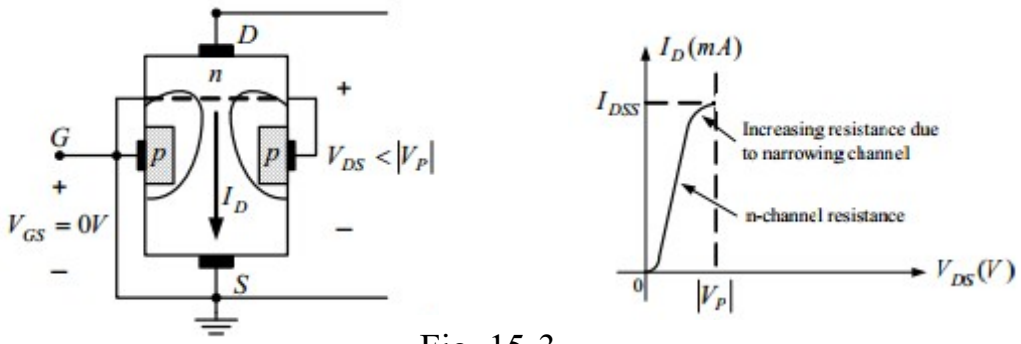


Fig. 15-3

- When $V_{GS} = 0$ V and ≥ VV_{PDS} : I_D remains at its saturation value I_{DSS} beyond V_P, as shown in Fig. 15-4.

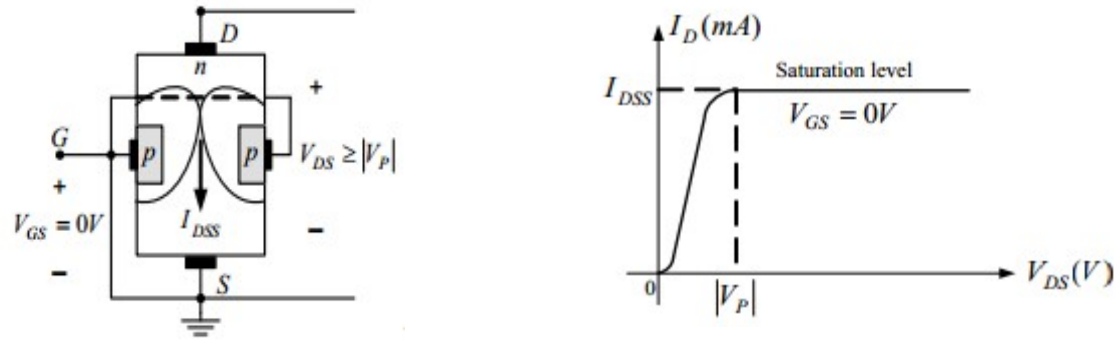


Fig. 15-4

- When $V_{GS} < 0$ and V_{DS} some positive value: The effect of the applied negative-bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0$ V but at lower levels of V_{DS}. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at lower level of V_{DS}, as shown in Fig. 15-5.

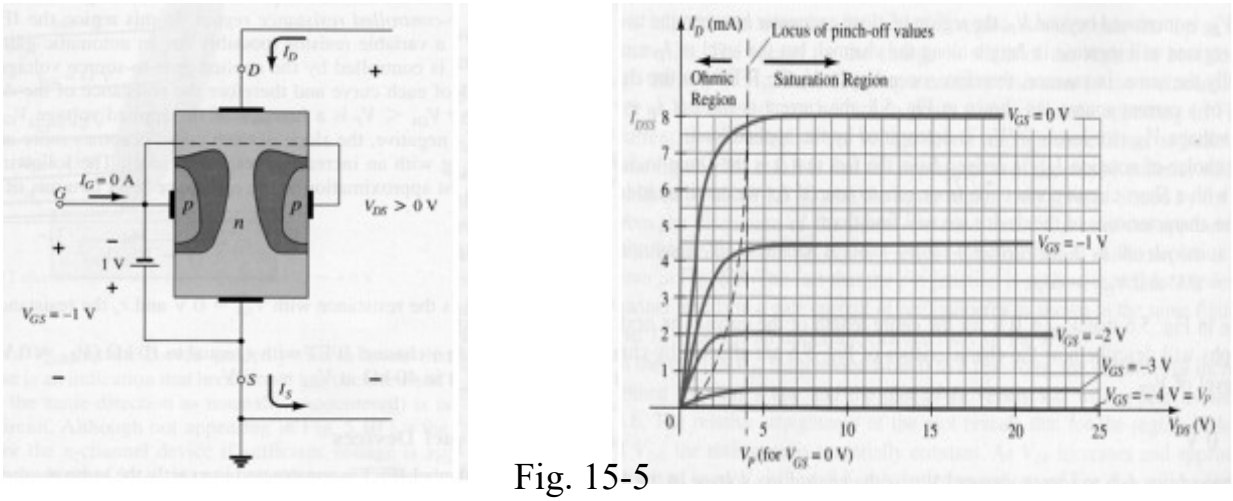


Fig. 15-5

Summary:

For n-channel JFET:

1. The maximum current is defined as I_{DSS} and occurs when $V_{GS} = 0$ V and $\geq VV_{PDS}$ as shown in Fig. 15-6a.
2. For gate-to-source voltages V_{GS} less than (more negative than) the pinch-off level, the drain current is 0 A ($I_D = 0$ A) as appearing in Fig. 15-6b.
3. For all levels of V_{GS} between 0 V and the pinch-off level, the current I_D will range between I_{DSS} and 0 A, respectively, as shown in Fig. 15-6c.

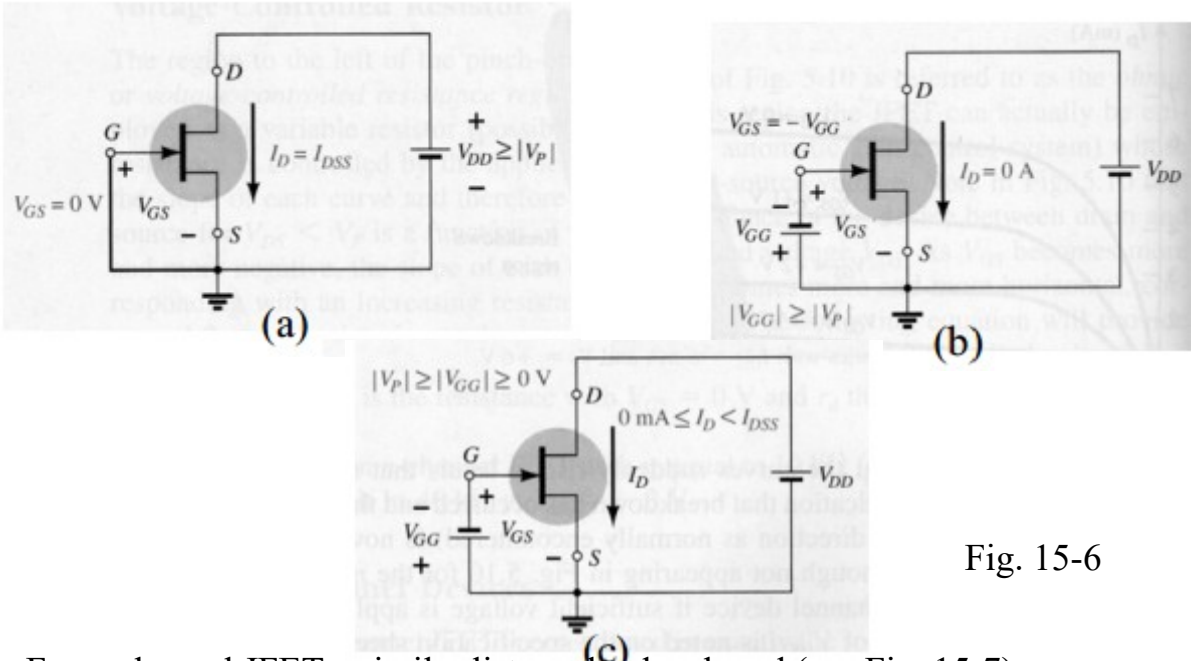


Fig. 15-6

For p-channel JFET a similar list can be developed (see Fig. 15-7)

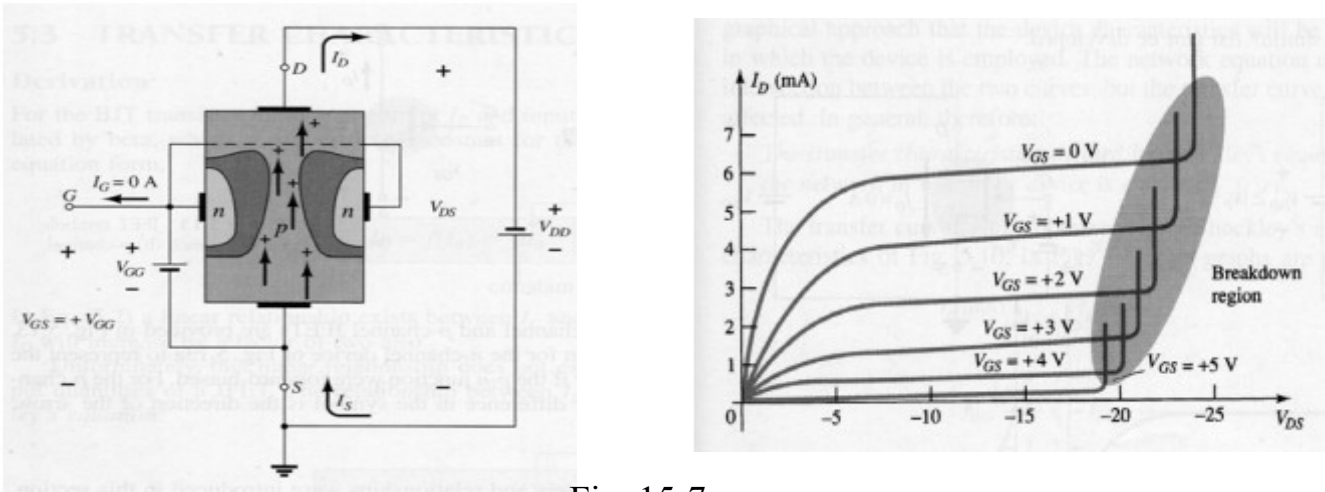


Fig. 15-7

Shockley's Equation:

For the BJT the output current I_C and input controlling current I_B were related by β, which was considered constant for the analysis to be performed. In equation form:

Control variable ↓

$$I_C = \beta I_B$$

↑ constant

In the above equation a linear relationship exists between I_C and I_B.

Unfortunately, this linear relationship does not exist between the output (I_D) and input (V_{GS}) quantities of a JFET. The relationship between I_D and V_{GS} is defined by Shockley's equation:

Control variable ↓

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

↑ ↑ constant

The squared term of the equation will result in a nonlinear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitude of V_{GS}.

Transfer Characteristics:

Transfer characteristics are plots of I_D versus V_{GS} for a fixed value of V_{DS}. The transfer curve can be obtained from the output characteristics as shown in Fig. 15-8, or it can be sketched to a satisfactory level of accuracy (see Fig. 15-9) simply using Shockley's equation with the four plot points defined in Table 15-1.

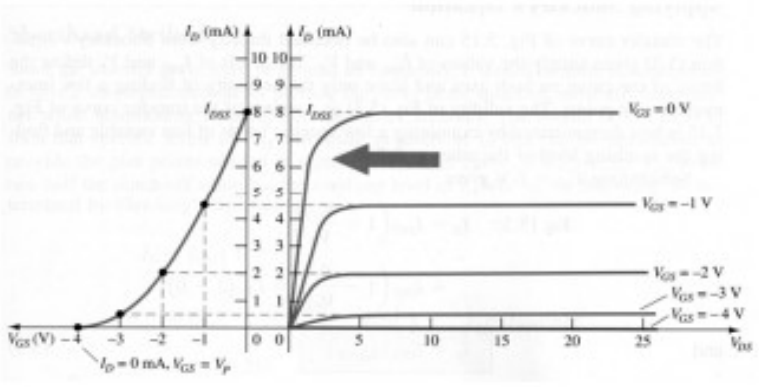


Fig. 15-8

Table 15-1

$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$	
V_{GS} (V)	I_D (mA)
0	I_{DSS}
$0.3\,V_P$	$I_{DSS}/2$
$0.5\,V_P$	$I_{DSS}/4$
V_P	0

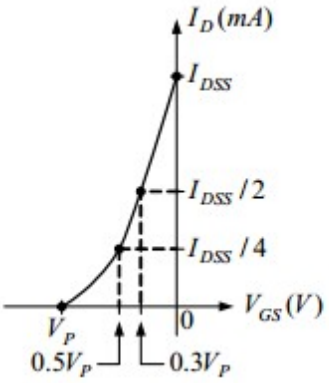


Fig. 15-9

Important Relationships:

A number of important equations and operating characteristics have introduced in the last few sections that are of particular importance for the analysis to follow for the dc and ac configurations. In an effort to isolate and emphasize their importance, they are repeated below next to a corresponding equation for the BJT. The JFET equations are defined for the configuration of Fig. 15-10a, while the BJT equations relate to Fig. 15-10b.

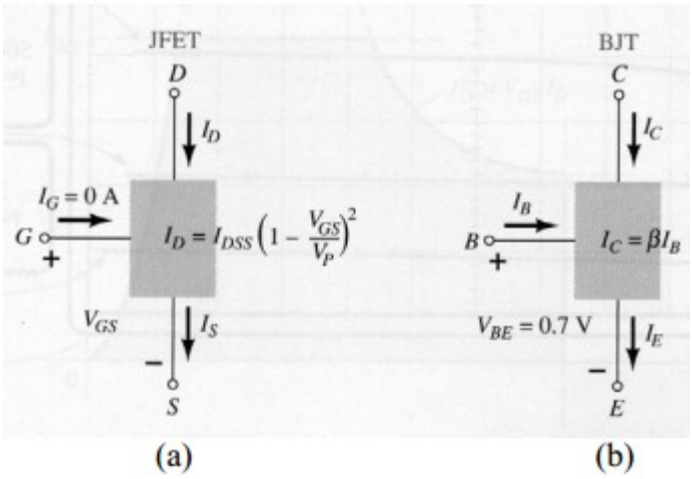


Fig. 15-10

JFET **BJT**

$$I_D \approx I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \Leftrightarrow I_C \approx \beta I_B$$

$$I_D \approx I_s \Leftrightarrow I_C \approx I_E$$

$$I_D \cong 0\,A \Leftrightarrow V_{BE} \cong 0.7V$$

Transconductance Factor:

The change in drain current that will result from a change in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\Delta I_D = g_m . \Delta V_{GS}$$

The transconductance factor, g_m, (on specification sheets, g_m is provided as y_{fs}) is the slop of the characteristics at the point of operation, as shown in Fig. 15-11. That is,

$$g_m = y_{fs} = \left(\frac{\Delta I_D}{\Delta V_{GS}}\right), at\ V_{GS} = const.$$

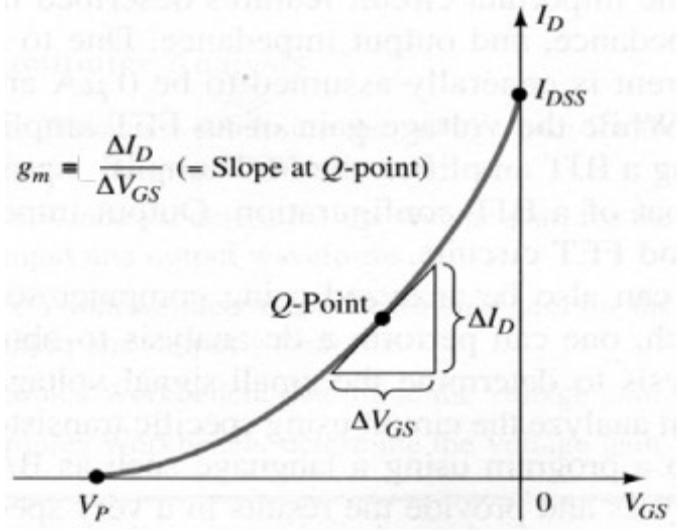


Fig. 15-11

An equation for g_m can be derived as follows:

$$g_m = \left(\frac{d I_D}{d V_{GS}}\right), at\ Q_{pt.} = \frac{d}{d V_{GS}} I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\frac{d}{d V_{GS}}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$g_m = 2 I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)\frac{d}{d V_{GS}}\left(1-\frac{V_{GS}}{V_P}\right) = 2 I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)\left(0-\frac{V_{GS}}{V_P}\right)$$

$$g_m = \frac{2 I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right) \qquad [15.2]$$

And

$$g_{mo} = \frac{2 I_{DSS}}{V_P} \qquad [15.3]$$

where is the value of g_m at $V_{GS} = 0$ V.g_{mo}
Equation [15.2] then becomes:

$$g_m = g_{mo}\left(1-\frac{V_{GS}}{V_P}\right) \qquad [15.4]$$

JFET Output Impedance:

The output impedance (r_d) is defined on the drain (output) characteristics of Fig. 15-12 as the slope of the horizontal characteristic curve at the point of operation.
In equation form:

$$r_d = \frac{1}{y_{os}} = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|, \text{at } V_{GS} = const. \qquad [15.5]$$

where y_{os} is the output admittance, with the units of μS, as appear on JFET specification sheets.

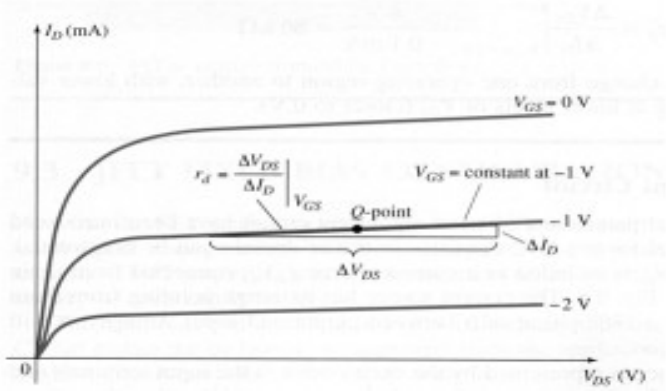


Fig. 15-12

JFET AC Equivalent Circuit:

The control of I_d by V_{gs} is include as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 15-13. The current source has its arrow pointing from drain to source to establish a 180_o phase shift between output and input voltages as will as occur in actual operation. The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source.

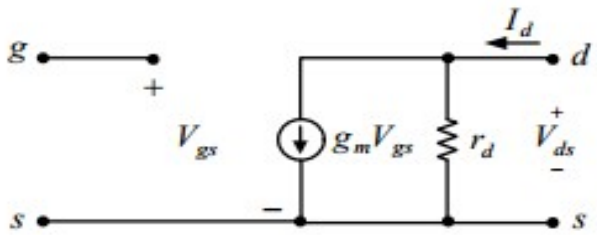


Fig. 15-13

Exercises:

1. Sketch the transfer curve defined by $I_{DSS} = 12$ mA and $V_P = -6$ V.

2. For a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ V, determine:
   a. the maximum value of g_m (that is,g_{mo}), and
   b. the value of g_m at the following dc bias points:
   $V_{GS} = -0.5$ V, $V_{GS} = -1.5$ V, and $V_{GS} = -2.5$ V.

3. Given $y_{fs} = 3.8$ mS and $y_{os} = 20$ μS, sketch the JFET ac equivalent model.