BJT Switching Circuits

Basic Concepts:

.The application of transistors is not limited solely to the amplification of signals .Through proper design it can be used as a switch for computer and control applications .The circuit of Fig. 11-1a can be employed as an **inverter** in computer logic circuitry .Note that the output voltage V_C is opposite to that applied to the base or input terminal In addition, note the absence of a dc supply connected to the base circuit. The only dc source is connected to the collector or output side and for computer applications is .typically equal to the magnitude of the "high" side of the applied signal-in this case 5V

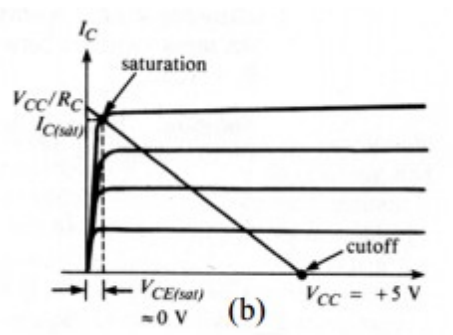


Fig. 11-1

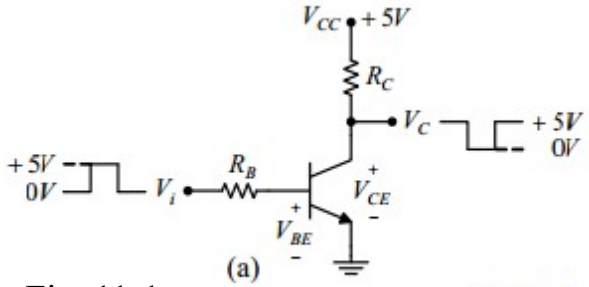


Fig. 11-1

Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line depicted in Fig. 11-1b. For our purposes we will assume that $I_C \approx I_{CEo} \approx 0$ mA when $I_B = 0$ μA (an excellent approximation in light of improving construction techniques), as shown in Fig. 11-1b. In addition, we will assume that $V_{CE} \approx V_{CE_{sat}} \approx 0\,V$ rather than the typical 0.1 to 0.3 V level.

When $V_i = 5$ V, the transistor will be "on" and the design must ensure that the circuit is heavily saturated by a level of I_B greater than that associated with the I_B curve appearing near the saturation level.

The base current I_B for the circuit of Fig. 11-1a is determined by

$$I_B = \frac{V_i - V_{BE}}{R_B} \qquad [11.1]$$

The saturation level for collector current $I_{C(sat)}$ for the same circuit is defined by

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} \qquad [11.2]$$

The level of I_B in the active region just before saturation results can be approximated by the following equation:

$$I_{B(max)} \approx \frac{I_{C(sat)}}{\beta} \qquad [11.3]$$

For the saturation level we must therefore ensure that the following is satisfied:

$$I_B \geq I_{B(max)} \qquad [11.4]$$

Example 11-1:

Verify that the circuit shown in Fig. 11-2 behaves like an inverter when the input switches between 0 V and +10 V. Assume that the transistor is silicon and that $\beta = 50$.

Solution:

It is only necessary to verify that the transistor is saturated when $V_i = +10$ V.

$$I_B = \frac{V_i - V_{BE}}{R_B} = \frac{10 - 0.7}{220\,k} = 42.3\,\mu A$$

$$I_{B(max)} = \frac{I_{C(sat)}}{\beta} = \frac{V_{CC}}{\beta R_c} = \frac{10}{(50)(6.2\,k)} = 32.3\,\mu A.$$

Thus, we have $I_B \geq I_{B(max)}$, therefore the transistor is saturated, and the circuit is inverter.

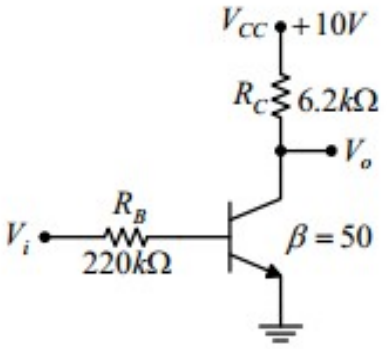


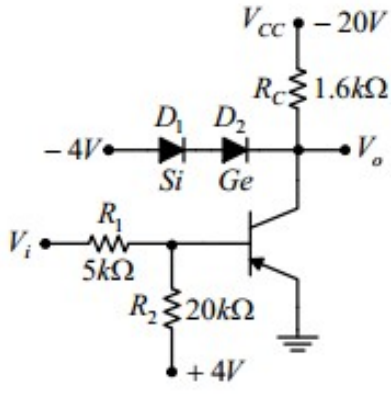
Fig. 11-2

Example 11-2:

Verify that the circuit shown in Fig. 11-3 is an inverter when the input switches between 0 V and -5 V. What minimum value of β is require transistor is silicon.

Solution:

$$when\ V_i = 0\,V,\ V_B = \frac{(4)(5\,k)}{20\,k \parallel 5\,k} = 0.8\,V,$$ hence the



transistor is at cutoff, so that D_1 and D_2 are on and

$V_o = -4 - 0.7 - 0.3 = -5\,V$.

when $V_i = -5\,V$, $R_{Th} = 5\,k \parallel 20\,k = 4\,k\Omega$

$$E_{Th} = \frac{4 \times 5\,k}{20\,k + 5\,k} + \frac{-5 \times 20\,k}{20\,k + 5\,k} = -3.2\,V$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th}} = \frac{3.2 - 0.7}{4\,k} = 625\,\mu A$$

Fig. 11-3

We assume the transistor is at saturation, $V_o = 0\,V$,

so that D_1 and D_2 are off and

$$I_{C(sat)} = \frac{V_{CC}}{R_c} = \frac{20}{1.6\,k} = 12.5\,mA$$

$$I_{B(max)} = \frac{I_{C(sat)}}{\beta} = 12.5\,mA / \beta$$

For the transistor to be in saturation,

$$I_B \geq I_{B(max)} \Rightarrow \beta \geq \frac{I_{C(sat)}}{I_B} = \frac{12.5\,m}{625\,\mu} = 20.$$

Exercise:

1. Design the transistor inverter of Fig. 11-4 to operate with a saturation current of 8 mA using a transistor with a beta of 100. Use a level of I_B equal to 120% of $I_{B(max)}$ and standard resistor values.

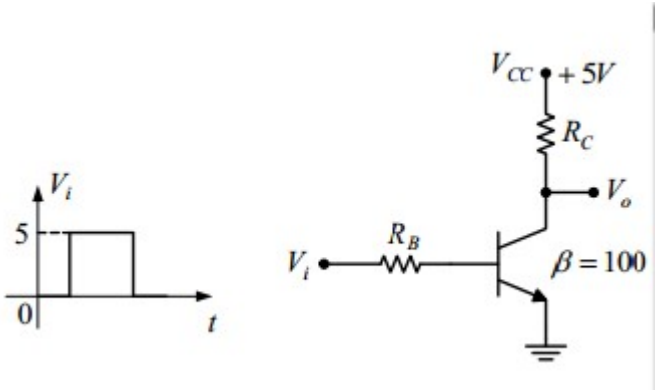


Fig. 11-4

2. Verify that the circuit shown in Fig. 11-5 is a positive NAND when the input switches between 0 V and +12 V. Neglect source impedance and junction saturation voltages and diode voltages in forward direction. Find the minimum value of β.

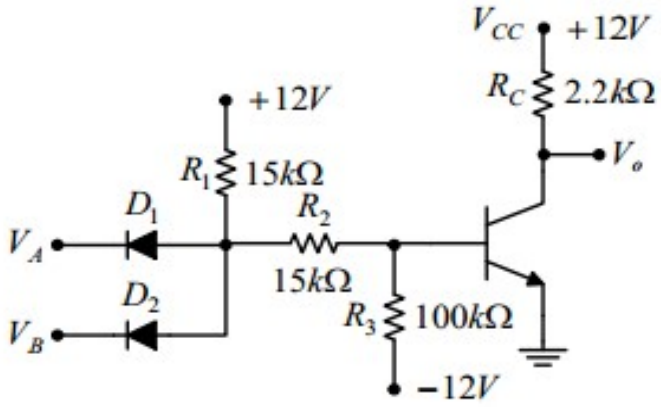


Fig. 11-5